



ARM Core
MPCore Test Chip (MP003)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r0p0 of MP003

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General suggestion for additions and improvements are also welcome.

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Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

22 Mar 2005: Changes in Document v12

Page	Status	ID	Cat	Summary
9	New	345141	Cat 2	L220 can deadlock when an internal 'cache sync' is issued
11	New	345140	Cat 3	MBIST testing of L220 Data RAM only possible with latency 0

Errata Summary Table

This document contains the errata specific to the test chip implementation (MP003). Note that the MPCore Test Chip inherits all the errata from the MPCore revision implemented in the test chip. Errata for MPCore are catalogued separately in the MPCore (MP002) Errata Notice (Connect Part Number: **MP002-DC-11001**)

The errata associated with this product affect product versions as below.

A cell shown thus

X

 indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0-05RELO
345141	Cat 2	L220 can deadlock when an internal 'cache sync' is issued	X
345140	Cat 3	MBIST testing of L220 Data RAM only possible with latency 0	X

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

345141: L220 can deadlock when an internal 'cache sync' is issued

Status

Affects: product MP003.

Fault status: Cat 2, Present in: r0p0-05REL0, Open. New in this document.

Description

The issue occurs when an L2 cache read and a write are performed simultaneously on the same port, at the same time as a L2 cache maintenance operation which causes a Cache Sync. If the Cache Sync occurs simultaneous with the read and the write, the line read buffer (LRB) is invalidated incorrectly, causing the data for the read operation to never be returned. Thus this causes a lock-up situation.

Implications

It is possible to deadlock the MPCore Testchip.

Workaround

1. Use the SCU in twin master port mode. Then, use an OS API to 'stop all CPUs', before using a SWP instead of a STR for all L220 cache maintenance operations.

Robust solution that has been demonstrated with SMP Linux 2.6.7

2. Enable and use L220 as normal. This is a testchip, and the scenario is difficult to produce. Accept occasional lockups and reset.

Not a robust solution. However, this may be acceptable if using the TestChip to develop software, as any product which includes MPCore and L220 will have the fixed L220, so this would avoid any software re-work.

3. Use the SCU in single master port mode. ie. MPCore -> L220, single master; L220 -> TestChip IO, single or dual master Then, use a SWP instead of a STR for all L220 cache maintenance operations.

Robust solution, as the SWP read reads the cache maintenance register and drains all L220 buffers, then locks the read port whilst the SWP write is completed. The internal 'cache sync' now completes before the read port LRB can be reloaded for a subsequent read.

4. Bypass L220

Robust solution, but performance will suffer.

5. Do not enable L220

Robust solution, but performance will suffer.

Errata - Category 3

345140: MBIST testing of L220 Data RAM only possible with latency 0

Status

Affects: product MP003.

Fault status: Cat 3, Present in: r0p0-05REL0, Open. New in this document.

Description

It has been found that the MBIST controller drives the address out to the L220 Data RAM and is valid only for the clock cycles when the CS is asserted. There is a 'way selector mux' driven by the address to select the output from one of ways 0-7. Consequently, when the latency is more than 0, as the address out from the MBIST controller reverts back to 0 after the initial access cycle, the 'way selector mux' reverts back to way 0, so the wrong data is read back to the MBIST controller.

Implications

L220 DATA RAMs can only be tested through MBIST if the DATA RAM latency is set to 0. The L220 Tag and Dirty RAM can be tested correctly by the MBIST controller on all latencies.

Functional operation is not affected, as the address is driven valid throughout the duration of the access by the L220.

Workaround

A work-around is only needed if DATA RAM latency has to be higher than 0 at TestChip full speed. In that case, the only way to test DATA RAMs through MBIST is to set DATA RAM latency to 0 in the MBIST controller and to perform MBIST test at lower frequency.

Errata - Documentation

There are no Errata in this Category

Errata – Driver Software

There are no Errata in this Category